

# PhotonHub Experience Centre

Course **xx**

Silicon and Silicon Nitride Photonic Integrated Circuits

## Course Provider

ePIXfab – the European Silicon Photonics Alliance  
and its members

Hosted from Ghent University, Belgium

# Course Overview

Silicon photonics (SiPh) is a key photonic integration technology. The evolution pace of silicon photonics technology is tremendous. Industries developing SiPh-based solutions have to continuously train their workforce to equip them with latest trends and developments.

This 3-day training course provides industry, especially those involved in PIC-based product development, with the basic technical skills in ideating, designing, fabricating and testing SiPh PICs. The course covers various forms of SiPh such as thin SOI, thick SOI, LPCVD SiN, PECVD SiN, and Ge- on-Si along with the deployment of these technologies into application domains such as communications, medical, sensors, quantum, environmental, computing, etc.

The training will be organized by ePIXfab (hosted by UGent) with the support of its members that are partners in PhotonHub Europe project. The support provided by ePIXfab members will make the course cohesive and inclusive to all forms and brands of SiPh technologies – that is the biggest value proposition of the proposed course and makes it unique in the European landscape.

The training will provide a hands-on training with respect to:

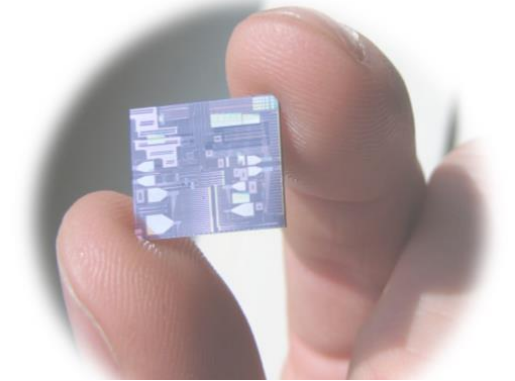
- determining the right SiPh technology platform & design environment for a given application
- designing a SiPh chip and associated key fabrication steps
- developing test-beds and testing of SiPh PICs for various applications.

# Target Audience

It is desirable but not essential that course attendees have a basic understanding of photonics. The course is ideally suited to those planning to internalize basic skills necessary for innovative PIC-based product development.

## Expected Outcomes

- 1) Mastery in choosing the appropriate technology platform for a use case
- 2) Mastery in adopting the right design framework for a use case
- 3) Hands-on skills with respect to the SiPh design process
- 4) Understanding of challenges associated with the fabrication of SiPh chips
- 5) Experience in different testing schemes and fiber-chip-fiber coupling schemes
- 6) Experience in on-chip opto-electronic testing, including high speed testing



# Course Equipment & Infrastructure



Design Software  
(Device, Circuit, Layout, System)

4.3.5 RFC

Rule code	Value	Description
RFC.W.1	0.100	Minimum width on RFC layers
RFC.S.1	0.100	Minimum spacing on RFC layers
RFC.ANGLEDGE		Acute angle -45° is illegal
RFCCLD.E.RFCCOR	0.100	Minimum cladding enclosure of core
RFCTRE.IO.RFCHOL		Illegal Overlap between trenches and holes
RFCCLD.IO.RFCHOL		Illegal Overlap between cladding and holes
RFC.IO.LOCKOUT		Illegal Overlap between LOCKOUT and RFC layers
RFCCOR.S.SAL	1.0	R. Minimum spacing between SAL and RFC core
RFCCOR.S.NPLUS	1.0	R. Minimum spacing between NPLUS and RFC core
RFCCOR.S.PPLUS	1.0	R. Minimum spacing between PPLUS and RFC core

4.3.6 PBODY,NBODY

The diagram shows two cross-sectional views of waveguide structures. The left view is labeled 'FCW\_COR' and shows a core layer on a substrate. The right view is labeled 'FCW\_COR' and 'WAG\_TRE' and shows a core layer with a trench. Below the diagrams, the text 'Poly rib waveguide (FCW)' and 'Poly-only waveguide' is visible.

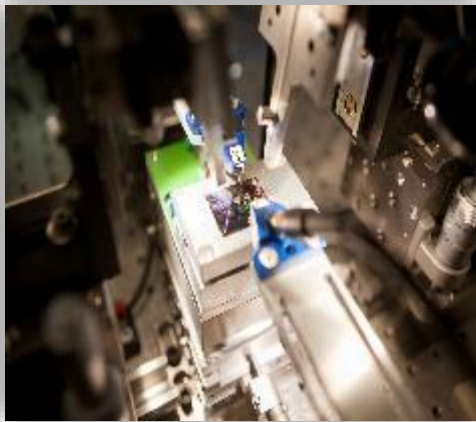
4.3.0 PFC,PLL

Rule code	Value	Description
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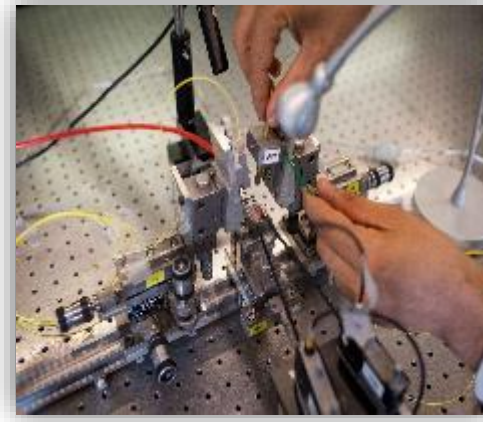
Fab-like PDKs



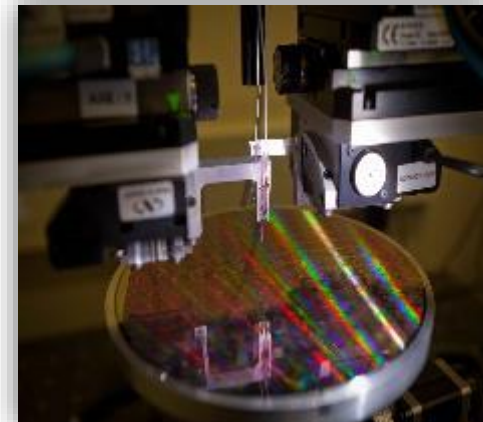
Cleanroom processes



High-speed test beds



Vertical and horizontal  
coupling setups



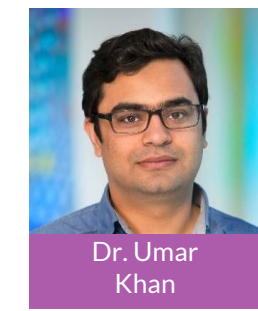
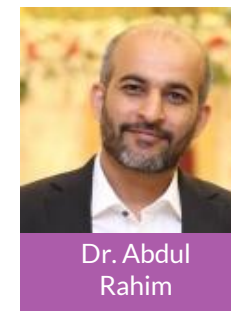
Wafer-level automated  
testing setups

# Course Schedule

Day	Time	Training Activity
DAY 1	09:00 – 10:00	Welcome + Introduction to silicon photonics (tutorial)
	10:30 – 12:30	Basics of silicon photonics designs (hands-on)
	1:30 – 5:30	Design your silicon photonics circuit on a chip (hands-on)
DAY 2	09:00 – 10:00	Silicon photonics chip fabrication in a CMOS fab (tutorial)
	10:30 – 12:30	Exposure to different silicon photonics platforms (demos + hands-on)
	1:30 – 4:30	Fabricating a silicon photonics chip (Hands-on)
	5:00 – 6:00	Laser co-integration with silicon photonics (tutorial)
DAY 3	09:00 – 12:30	Learn to couple light into a chip from a fiber for different application wavelengths, thermal tuning and passive device characterization on your own fabricated chip (demos + hands-on)
	13:30 – 17:00	Learn to test an unpackaged silicon/silicon nitride PICs for various application areas (demos + hands-on)
	17:30 – 18:30	Digital meetup and Q&A with fab experts (online – on request)

# Program: Day 1

**Module:**  
**Learn how to design a silicon photonic integrated circuit**



Element	Speaker/Trainer	Where?	When?
Welcome	Roel Baets	Room Allan Turing , iGent Tower, Floor 1	09:00 – 09:10
Program and Housekeeping	Abdul Rahim		09:10 - 09:20
Short introduction to silicon photonics	Wim Bogaerts		09:20 – 10:00
Tutorial: <ul style="list-style-type: none"> <li>• Concept of process design kit (PDK)</li> <li>• How to design silicon photonic ICs?</li> <li>• Compact models and circuit simulations</li> </ul>	Umar Khan		10:00 – 10:30
Hands-on: Designing a simple silicon photonic IC	Umar Khan		10:30 – 12:30
Hands-on: Designing a simple silicon photonic IC	Umar Khan		1:30 – 5:15
Quiz	Umar Khan		5:15 – 5:30



Available in the meeting room



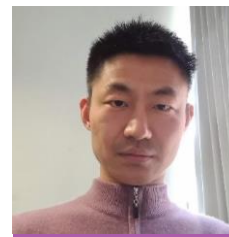
12:30 – 1:30 PM at Floor 12



# Program: Day 2

## Module:

Learn how to design a silicon photonic integrated circuit



Dr. Dongbo Wang



Dr. Nuria Teigel Benítez



Mr. Muhammad Muneeb



Ms. Liesbet Van Landschoot



Prof. Gunther Roelkens

Element	Speaker/Trainer	Where?	When?
Tutorial: Overview of silicon photonics chip fabrication in a CMOS fab	Dongbo Wang	Room Allan Turing , iGent Tower, Floor 1	09:00 – 10:00
Demos: <ul style="list-style-type: none"> <li>Clean room safety</li> <li>Exposure to different silicon photonics platforms</li> </ul>	Muhammad Muneeb, Nuria Teigell Beneitez	Tech. Park building 123 (Clean room building)	10:30 – 12:00
Hands-on: <ul style="list-style-type: none"> <li>Sample preparation (cleaving, cleaning, spin-coating)</li> <li>E-beam exposure of the design from Day 1</li> <li>Reactive ion etching of the exposed and developed samples</li> </ul>	Muhammad Muneeb, Nuria Teigell Beneitez, Dongbo Wang, Liesbet Van Landschoot	Tech. Park building 123 (Clean room building)	1:00 – 4:30
Tutorial: Laser co-integration with silicon photonics	Gunther Roelkens	Room Allan Turing , iGent Tower, Floor 1	5:00 – 6:00
Quiz			6:00 – 6:15
Group Dinner		In a local Ghent Restaurant	7 PM – 10 PM



Available in the meeting room



12:30 – 1:30 PM at Floor 12

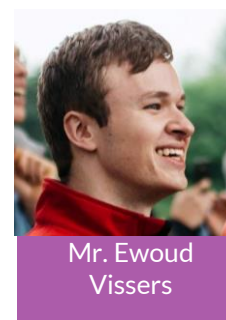
# Program: Day 3

## Module:

### Learn how to characterize a silicon photonic integrated circuit



Dr. Jing Zhang



Mr. Ewoud Vissers



Mr. Hong Deng



Dr. Maximilien Billet



Dr. Laurens Bogaert

Element	Speaker/Trainer	Where?	When?
<p>Hands-on:</p> <ul style="list-style-type: none"> <li>Execute and optimize coupling of light in and out of a chip, both horizontally and vertically (single fiber or fiber array) for different application wavelengths                             <ul style="list-style-type: none"> <li>Execute the measurement of a simple silicon photonic circuit (for example, a ring resonator or an MZI)</li> <li>Test a PIC with optical and low-speed electrical probing (for example, by using thermal heaters)</li> </ul> </li> </ul>	Jing Zhang, Ewoud Vissers, Hong Deng	Measurement rooms, iGent Tower, Floor 4 Scheme: - By dividing the participants into three groups and rotating them among the three hands-on sessions	09:00 – 12:30
<p>Hands on:</p> <ul style="list-style-type: none"> <li>Test a PIC with optical and high-speed electrical probing</li> <li>Characterization of a laser integrated on a silicon photonics chip</li> </ul>	Laurens Bogaert, Maximilien Billet	Measurement rooms, iGent Tower, Floor 4	1:30 – 4:30
<p>Demo:</p> <ul style="list-style-type: none"> <li>analyze the measured data for chip fabricated on Day 2</li> </ul>			4:30 – 5:00
Quiz			5:00 – 5:15



Available in the meeting room



12:30 – 1:30 PM at Floor 12



# Course Trainers

**Course Directors: Prof. Roel Baets, Prof. Wim Bogaerts**

**Course Manager: Dr. Abdul Rahim**

**Tutorials: Selected speakers from PhotonHub , Experts from UGent- ePIXfab**

**Chip Fabrication: UGent Cleanroom staff**

**Chip Coupling: ePIXfab + UGent Manpower + Application engineers from PhotonHub partners**

**Chip Testing: ePIXfab + UGent Manpower + Application engineers from PhotonHub partners**

# Course Material (technical hand-outs)



- **Electronic access to**
  - **Course handouts/slides**
  - **Video recordings of tutorials**
  - **Design examples**
  - **Python notebooks**
  - **Video recordings of lab demos**

<https://einstein.epixfab.eu>

# Course Location, Schedule & Cost

- Course Location: Ghent, Belgium
- Course Schedule (exact dates to be confirmed)
- Number of people (Groups of 10 people per course)
- Course Cost (500 Euros per person, includes lunch catering, handouts, etc.)

## Further Information

- [abdul.rahim@epixfab.eu](mailto:abdul.rahim@epixfab.eu)
- <https://epixfab.eu>
- [www.photonhub.eu/euphotonicsacademy](http://www.photonhub.eu/euphotonicsacademy)



UGent  
Cleanroom



Technologiepark-Zwijnaarde 126  
9052 Gent



At the heart  
of Europe

# Keywords

**Silicon photonics, SOI, Silicon Nitride, High Index Contrast, CMOS, Laser, Modulators, Detectors, Component design, Circuit simulation, System emulation, Design layout, Design Rules, Manufacturing, Pilot Line, Ecosystem, Open-access, Fabless, Fab-lite, Communications, Medical, Sensors, Quantum, Environmental, Computing**