PhotonHub Demo Centre

Thick-SOI photonics for sensing and imaging

Course Provider

VTT Technical Research Centre of Finland Ltd., Finland

Course Overview

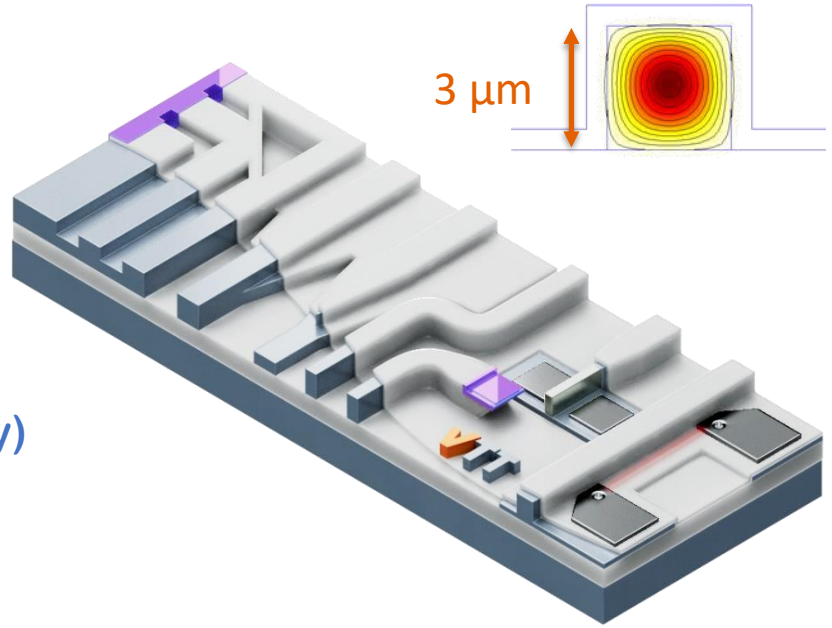
Photonic integrated circuits (PICs) can be realized on many different technology platforms and used for numerous different applications. This course focuses on the so-called Thick-SOI platform and its use for sensing and imaging applications in the near and mid-infrared region. Primary focus is on 3 µm thick silicon-on-insulator (SOI) waveguide technology, which is the most mature PIC technology platform at VTT. This platform is also available for small-to-medium volume contract manufacturing via VTT, and there is path to large-volume manufacturing via VTT's partners. Process design kits are available in multiple PIC design software platforms.

This one-day hands-on training course provides industry an overview of the Thick-SOI PIC platform and its feasibility in sensing and imaging applications. A clean room tour in Micronova offers an overview of the used fabrication methods and facilities. Hands-on training includes 1) the design of 3 µm SOI PICs using PIC design software, 2) General cleanroom visit and introduction to state-of-the-art manufacturing tools, and 3) PIC testing in the photonics measurement lab. The last part includes semi-automated fiber-to-waveguide alignment, optical beam steering with an optical phased array (OPA) and testing of other silicon photonic chips.

Target Audience

It is desirable but not essential that course attendees have a basic understanding of photonics. The course is ideally suited to those planning to develop new photonic products based on low-loss photonic integrated circuits (PICs) operating within the 1.2-6.0 µm wavelength range where the thick (µm-scale) silicon-on-insulator (SOI) waveguides can operate.

Expected Outcomes

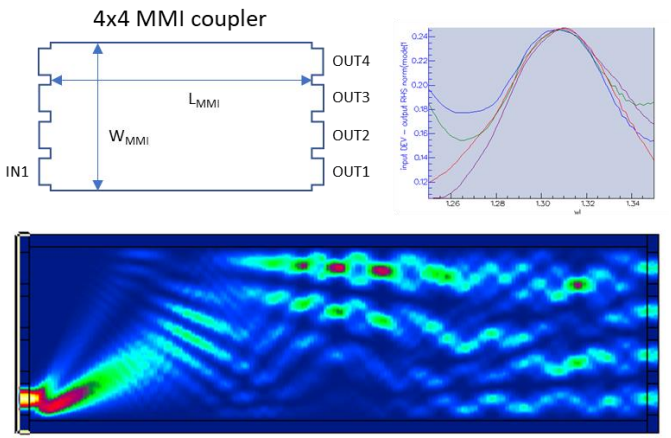


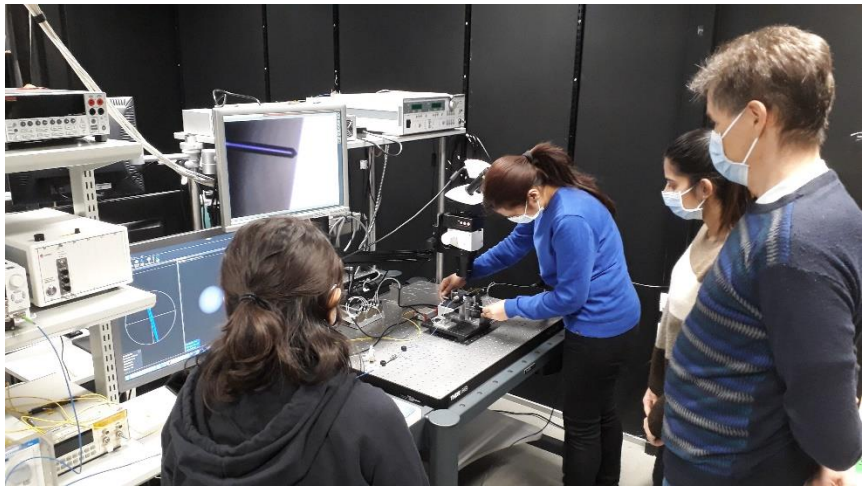
1) Understanding the technical advantages and limitations of Thick-SOI PIC technology, as well as its key applications
2) Learn how the Thick-SOI PICs are designed & simulated (hands-on activity)
3) See the fabrication process of 3 µm SOI PICs (visit to the clean room)
4) Learn how the Thick-SOI PICs are tested at chip-level (hands-on activity)
5) See demonstrations of 3 µm SOI PICs in imaging applications (hands-on activity)

Course Schedule

Time	Demo Activity
09:00 – 10:45	**Introduction to the course, to Thick-SOI technology and its main applications**
11:00 – 12:30	Demo 1: Design of 3 µm SOI PICs using a process design kit (hands-on)
12:30 – 13:30	Networking & Lunch
13:30 – 15:00	Demo 2: Clean-room visit to see fabrication flow (hands-on)
15:15 – 17:00	Demo 3: Chip-level testing and demonstration of Thick-SOI in sensing & imaging (hands-on)
17:00 – 17:30	**Follow-Up Questions & Close**

Course Trainers





Course Director: Timo Aalto

Course Manager: Srivathsa Bhat

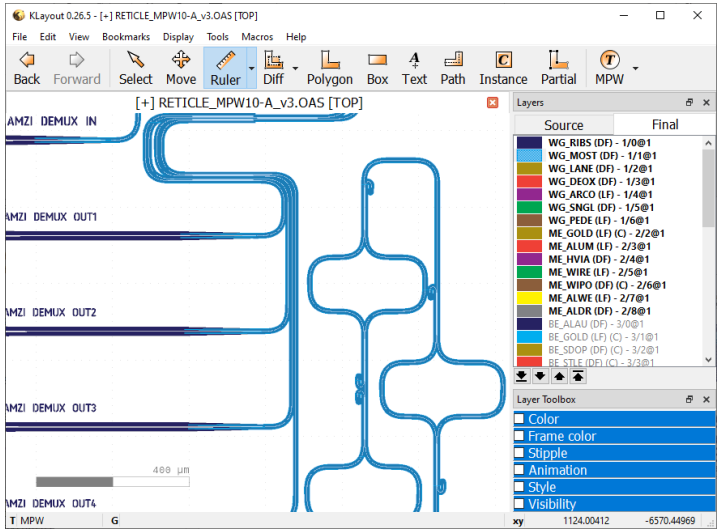
Demo 1: Mikko Harjanne (PIC design)

Demo 2 : Fei Sun (clean room visit)

Demo 3: Somnath Paul (chip-level testing and application demos)

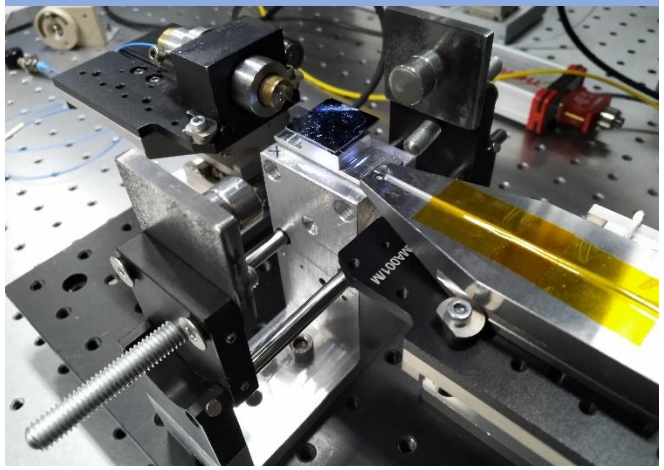
Course Demonstrators

PIC design demo

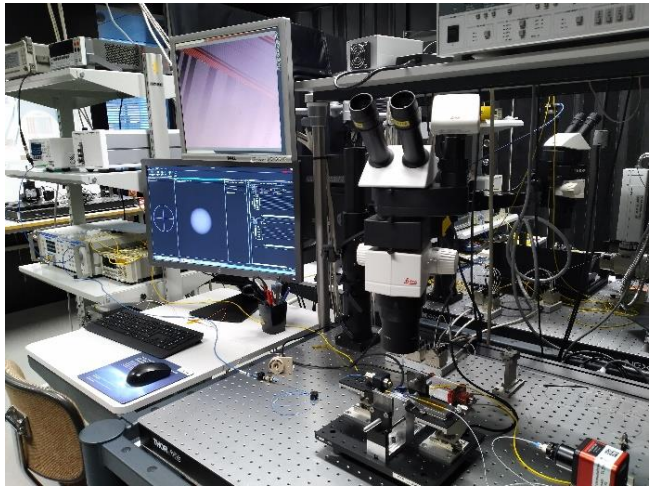


Clean room tour

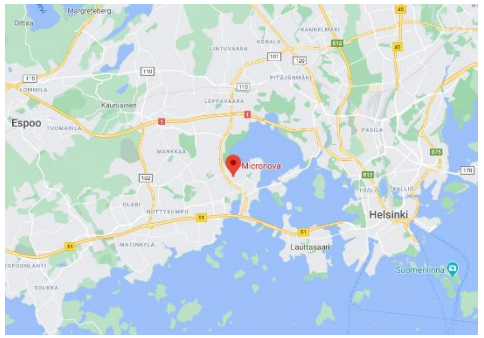
Fiber-PIC coupling demonstration



Optical sensing and imaging demonstrations



Course Location, Schedule & Fee



- Course location: VTT, Micronova, Tietotie 3, Espoo, Finland (few metro stops from downtown Helsinki)
- Course Date:
  - Training 1 – 27th May 2024
  - Training 2 – 31st May 2024
- Number of trainees: Maximum 10 people per course
- Course Fee (includes catering and project consumables):
  - Early-bird (registration before 15th April) - 100 € per person
  - Regular (registration after 15th April) - 200 € per person

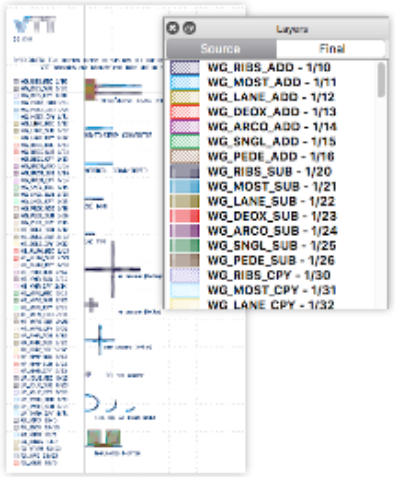
Further Information

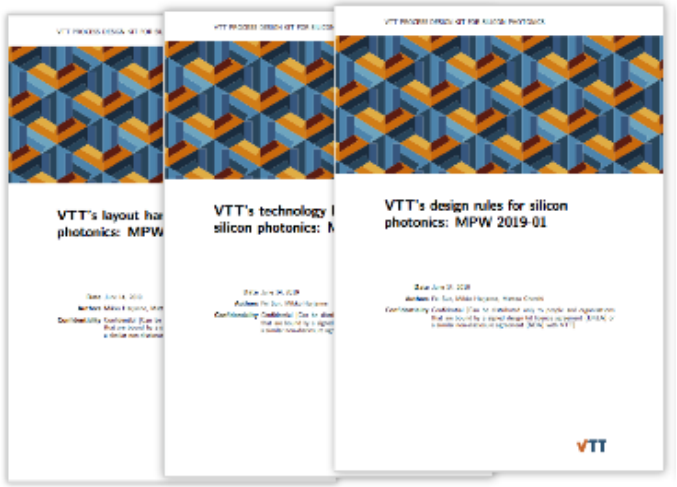
- Email: srivathsa.bhat@vtt.fi, timo.aalto@vtt.fi
- Training website: www.photonhub.eu/euphotonicsacademy
- VTT website: https://www.vttresearch.com/en

Course Material (technical hand-outs)

Digital course materials:

- Course instructions and notes
- Copies of slides
- Video recordings
- Process design kit (PDK) for 3 µm SOI PICs
  (some parts require a signed design kit license agreement)





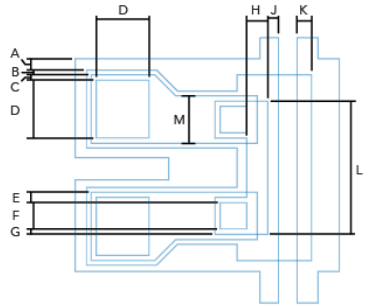


Figure 4.3: Mask parameters for the implanted heater.

Table 4.1: Parameter values related to Fig. 4.3.

Dimension	Description	Mask layer	Min.	Typical	Unit
A	Gap between wire and SOI sidewall	MR_WIRE	5.0	5.0	um
B	Distance between pedestal edge and metal	WG_PEDE	1.0	..	um
C	Gap between contact pad opening and metal edge	MR_WIPO	3.0	10.0	um
D	Size of contact pad opening	MR_WIPO	60	100.0	um
E	Heater via to wire edge distance	MR_HVIA	3.0	3.0	um
F	Size of heater via opening	MR_HVIA	5.0	5.0	um
G	Heater via to implantation edge distance	MR_HVIA	1.0	1.0	um
H	Implanted heater width	MP_PINP	3.0	4.0	um
J	Gap between implantation edge and waveguide	MP_PINP	2.0	2.0	um
K	Pedestal extension past waveguide edge	WG_PEDE	2.0	.	um
L	Implanted heater length	MP_PINP	..	100.0	um
M	Width of aluminium wire	MR_WIRE	5.0	7.0	um

Keywords

Integrated Photonics, PIC, PIC Design, PDK, Silicon-on-Insulator, SOI, Wafer Processing, Sensing, Imaging, Optical Phased Array, Optical Fiber, Laser, Testing, Test automation

Relevant Technology & Application Domain

Technology: Silicon photonics

Application: Relevant to all application domains, but course focuses on sensing and imaging